

References

1. Junior, A.A.C.; Misra, S.; Soares, M.S. A Maturity Model based on ISO/IEC/IEEE 42010:2011 to Identify Technical Debt in Software Architecture. In Proceedings of the International Conference on Computational Science and Its Applications (ICCSA), Saint Petersburg, Russia, 1–4 July 2019; pp. 31–42.
2. Wang, R.X.; Moon, S.H.; Hu, X.S.; Jiao, X.; Reis, D. A Computing-in-Memory-Based One-Class Hyperdimensional Computing Model for Outlier Detection. *IEEE Trans. Comput.* **2024**, *73*, 1559–1574.
3. Choi, H.-J.; Um, J.-Y. Design and HDL Implementation of Pulse-Arrival-Time Estimation Using XGBoost Regression with Tree-Recycling Architecture. *IEEE Access* **2025**, *13*, 27596–27609.
4. Li, G.H.; Mandal, S.K.; Ogras, U.Y.; Marculescu, R. FLASH: Fast Neural Architecture Search with Hardware Optimization. *ACM Trans. Embed. Comput. Syst.* **2021**, *20*, 63.
5. Kiaei, P.; Yao, Y.; Liu, Z.-Y.; Fern, N.; Breunese, C.-B.; Van Woudenberg, J.; Gillis, K.; Dich, A.; Grossmann, P.; Schaumont, P. Gate-Level Side-Channel Leakage Ranking with Architecture Correlation Analysis. *IEEE Trans. Emerg. Top. Comput.* **2024**, *12*, 496–507.
6. Fasfous, N.; Vemparala, M.R.; Frickenstein, A.; Valpreda, E.; Salihu, D.; Doan, N.A.V.; Unger, C.; Nagaraja, N.S.; Martina, M.; Stechele, W. HW-FlowQ: A Multi-Abstraction Level HW-CNN Co-design Quantization Methodology. *ACM Trans. Embed. Comput. Syst.* **2021**, *20*, 66.
7. Gagliardi, M.; Konrad, M.; Schmidt, D. *Addressing Open Architecture in Software Cost Estimation*; SEI Blog; Carnegie Mellon University: Pittsburgh, PA, USA, 2020.
8. Guertin, N.; Miller, R. A-RCI—The Right Way to Submarine Superiority. *Nav. Eng. J.* **1998**, *110*, 21–33.
9. Xin, Y.; Li, W.J.; Jia, C.J.; Li, X.F.; Xu, Y.; Liu, B.; Tian, Z.H.; Zhang, W.Z. Recursive Multi-Tree Construction with Efficient Rule Sifting for Packet Classification on FPGA. *IEEE/ACM Trans. Netw.* **2024**, *32*, 1707–1722.
10. Huzaifa, M.; Desai, R.; Grayson, S.; Jiang, X.T.; Jing, Y.; Lee, J.; Lu, F.; Pang, Y.H.; Ravichandran, J.; Sinclair, F.; et al. ILLIXR: An Open Testbed to Enable Extended Reality Systems Research. *IEEE Micro* **2022**, *42*, 97–106.
11. Jia, Q.; Cai, Y.; Çakmak, O.C. A Model-based, Quality Attribute-guided Architecture Re-Design Process at Google. In Proceedings of the 45th International Conference on Software Engineering: SEIP, Melbourne, Australia, 17–19 May 2023.
12. Open Systems Joint Task Force (OSJTF). *MOSA Program Assessment and Rating Tool*; OSJTF: Arlington, VA, USA, 2004.
13. Guertin, N.; Schmidt, D. A Modular Open Systems Approach (MOSA) Maturity Model. In Proceedings of the 21st Annual Acquisition Research Symposium, Monterey, CA, USA, 8–9 May 2024.
14. Open Architecture Assessment Team (OAET). *Naval Open Systems Architecture Strategy, Open Architecture Assessment Tool*; OAET: Patuxent River, MD, USA, 2014.
15. Office of the Under Secretary of Defense for Research and Evaluation (OUSD(R&E)). *DoD and Military Services MOSA Instructions and Guidance*; OUSD(R&E): Washington, DC, USA, 2022.
16. Silva, S.; Tuyishime, A.; Santilli, T.; Pelliccione, P.; Iovino, L. Quality Metrics in Software Architecture. In Proceedings of the IEEE 20th International Conference on Software Architecture Companion (ICSA-C), L'Aquila, Italy, 13–17 March 2023.
17. Beshley, M.; Kryvinska, N.; Beshley, H.; Panchenko, O.; Medvetskyi, M. Traffic engineering and QoS/QoE supporting techniques for emerging service-oriented software-defined network. *J. Commun. Netw.* **2024**, *26*, 99–114.
18. Li, G.H.; Mandal, S.K.; Ogras, U.Y.; Marculescu, R. FLASH: Fast Neural Architecture Search with Hardware Optimization. *ACM Trans. Embed. Comput. Syst.* **2021**, *20*, 63.
19. Cassano, L.; Iamundo, M.; Lopez, T.A.; Nazzari, A.; Di Natale, G. DETON: DEfeating hardware Trojan horses in microprocessors through software Obfuscation. *J. Syst. Archit.* **2022**, *129*, 102592.
20. Sarker, A.; Canto, A.C.; Kermani, M.M.; Azarderakhsh, R. Error Detection Architectures for Hardware/Software Co-Design Approaches of Number-Theoretic Transform. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2023**, *42*, 2418–2422.
21. Rajendran, S.R.; Dipu, N.F.; Tarek, S.; Kamali, H.M.; Farahmandi, F.; Tehranipoor, M. Exploring the Abyss? Unveiling Systems-on-Chip Hardware Vulnerabilities Beneath Software. *IEEE Trans. Inf. Forensics Secur.* **2024**, *19*, 3914–3926.
22. Smagulova, K.; Fouda, M.E.; Kurdahi, F.; Salama, K.N.; Eltawil, A. Resistive Neural Hardware Accelerators. *Proc. IEEE* **2023**, *111*, 500–527.
23. Ryu, D.; Kim, Y.; Hur, J. γ -Knife: Extracting Neural Network Architecture Through Software-Based Power Side-Channel. *IEEE Trans. Dependable Secur. Comput.* **2024**, *21*, 2686–2703.
24. Vo, Q.H.; Asim, F.; Alimkhanuly, B.; Lee, S.; Kim, L. Hardware Platform-Aware Binarized Neural Network Model Optimization. *Appl. Sci.* **2022**, *12*, 1296.
25. Bhaskar, C.V.; Munaswamy, P. An Efficient Reconfigurable Architecture for Software Defined Radio. *IEICE Trans. Inf. Syst.* **2023**, *106*, 1519–1527.
26. Wang, C.; Gong, L.; Li, X.; Yu, Q.; Wang, A.L.; Hung, P.T.; Zhou, X.H. SOLAR: Services-Oriented Deep Learning Architectures-Deep Learning as a Service. *IEEE Trans. Serv. Comput.* **2021**, *14*, 262–273.

27. Li, T.L.; Li, J.D.; Shen, G.B.; Zhao, D.C.; Zhang, Q.; Zeng, Y. FireFly-S: Exploiting Dual-Side Sparsity for Spiking Neural Networks Acceleration With Reconfigurable Spatial Architecture. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2024**, *72*, 4007–4020.
28. Mao, W.D.; Wang, M.Q.; Xie, X.R.; Wu, X.; Wang, Z.F. Hardware Accelerator Design for Sparse DNN Inference and Training: A Tutorial. *IEEE Trans. Circuits Syst. II Express Briefs* **2024**, *71*, 1708–1714.
29. Choi, H.-J.; Um, J.-Y. Design and HDL Implementation of Pulse-Arrival-Time Estimation Using XGBoost Regression with Tree-Recycling Architecture. *IEEE Access* **2025**, *13*, 27596–27609.
30. Beshley, M.; Kryvinska, N.; Beshley, H.; Panchenko, O.; Medvetskyi, M. Traffic Engineering and QoS/QoE Supporting Techniques for Emerging Service-Oriented Software-Defined Network. *J. Commun. Netw.* **2024**, *26*, 99–114.
31. Silva, M.; Gomes, T.; Ekpanyapong, M.; Tavares, A.; Pinto, S. ChamelloIoT: A tightly- and loosely-coupled hardware-assisted OS framework for low-end IoT devices. *Real-Time Syst.* **2024**, *60*, 150–196.
32. Hong, Y.; Ning, Z.H.; Sun, Y.; Shen, C.X. A dual-system trusted computing node construction method based on ARM multi-core CPU architecture. *Concurr. Comput. Pract. Exp.* **2022**, *34*, e7037.
33. Gruber, F.; Bandle, M.; Engelke, A.; Neumann, T.; Giceva, J. Bringing Compiling Databases to RISC Architectures. *Proc. VLDB Endow.* **2023**, *16*, 1222–1234.
34. Akgün, G.; Kolarov, B.; Kalberlah, H.; Wulf, C.; Willig, M.; Rettkowski, J.; Göhringer, D. Exploration of Power-Savings on Multi-Core Architectures with Offloaded Real-Time Operating System. *IEEE Access* **2024**, *12*, 11294–11315.
35. Liu, H.Z.; Luo, J.; Li, Y.; Wu, Z.H. Iterative Compilation Optimization Based on Metric Learning and Collaborative Filtering. *ACM Trans. Archit. Code Optim.* **2022**, *19*, 2.
36. Soto, J.E.; Hernández, C.; Figueroa, M. JACC-FPGA: A hardware accelerator for Jaccard similarity estimation using FPGAs in the cloud. *Future Gener. Comput. Syst.* **2023**, *138*, 26–42.
37. Denisov, L.; Galimberti, A.; Cattaneo, D.; Agosta, G.; Zoni, D. Design-time methodology for optimizing mixed-precision CPU architectures on FPGA. *J. Syst. Archit.* **2024**, *155*, 103257.
38. Kiaei, P.; Yao, Y.; Liu, Z.-Y.; Fern, N.; Breunese, C.-B.; Van Woudenberg, J.; Gillis, K.; Dich, A.; Grossmann, P.; Schaumont, P. Gate-Level Side-Channel Leakage Ranking with Architecture Correlation Analysis. *IEEE Trans. Emerg. Top. Comput.* **2024**, *12*, 496–507.
39. Sini, J.; Scialabba, K.; Violante, M.; Cosimi, F.; Arena, A. A Novel Approach to Address Random Hardware Failures for Automotive Application Within the ISO26262 and AUTOSAR Frameworks. *IEEE Access* **2024**, *12*, 165845–165860.
40. Nikulchev, E.; Ilin, D.; Kolyasnikov, P.; Magomedov, S.; Alexeenko, A.; Kosenkov, A.N.; Sokolov, A.; Malykh, A.; Ismatullina, V.; Malykh, S. Isolated Sandbox Environment Architecture for Running Cognitive Psychological Experiments in Web Platforms. *Future Internet* **2021**, *13*, 245.
41. Li, L.L.; Liu, J.Y.; Fan, J.P.; Qian, X.H.; Hwang, K.; Chung, Y.C.; Yu, Z.B. SOCA-DOM: A Mobile System-on-Chip Array System for Analyzing Big Data on the Move. *J. Comput. Sci. Technol.* **2022**, *37*, 1271–1289.
42. Javeed, K.; Gregg, D. Efficient Number Theoretic Transform Architecture for CRYSTALS-Kyber. *IEEE Trans. Circuits Syst. II Express Briefs* **2025**, *72*, 263–267.
43. Unal, D.; Falleni, S.; Enhos, K.; Demirors, E.; Basagni, S.; Melodia, T. Design and performance evaluation of SEANet, a software-defined networking platform for the Internet of Underwater Things. *Comput. Netw.* **2024**, *250*, 110579.
44. Liu, W.H.; Zhu, Z.W.; Li, B.Y.; Xiong, Y.; Lian, Z.R.; Geng, J.W.; Zhou, X.H. Arch2End: Two-Stage Unified System-Level Modeling for Heterogeneous Intelligent Devices. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2024**, *43*, 4154–4165.
45. Yacoub, M.H.; Ismail, S.M.; Said, L.A.; Madian, A.H.; Radwan, A.G. Reconfigurable hardware implementation of K-nearest neighbor algorithm on FPGA. *AEU-Int. J. Electron. Commun.* **2024**, *173*, 154999.
46. Chen, X.; Zhao, Y.T.; Guo, A.; Chen, J.W.; Dong, F.Y.; Zhang, Z.Y.; Xiong, T.Z.; Wang, B.; Kong, Y.Y.; Si, X. Toggle Rate Aware Quantization Model Based on Digital Floating-Point Computing-In-Memory Architecture. *IEEE Trans. Circuits Syst. II Express Briefs* **2024**, *71*, 3181–3185.
47. Mazumder, A.N.; Mohsenin, T. Reg-TuneV2: A Hardware-Aware and Multiobjective Regression-Based Fine-Tuning Approach for Deep Neural Networks on Embedded Platforms. *IEEE Micro* **2023**, *43*, 74–83.
48. Xu, H.; Bai, L.T.; Huang, W. An optimization-inspired intrusion detection model for software-defined networking. *Electron. Res. Arch.* **2025**, *33*, 231–254.
49. Lonbar, S.M.; Beigi, A.; Bagheri, N.; Peris-Lopez, P.; Camara, C. Deep learning based bio-metric authentication system using a high temporal/frequency resolution transform. *Front. Digit. Health* **2024**, *6*, 1463713.
50. Tuli, S.; Jha, N.K. EdgeTran: Device-Aware Co-Search of Transformers for Efficient Inference on Mobile Edge Platforms. *IEEE Trans. Mob. Comput.* **2024**, *23*, 7012–7029.
51. Kanso, H.; Noureddine, A.; Exposito, E. Automated power modeling of computing devices: Implementation and use case for Raspberry Pis. *Sustain. Comput. Inform. Syst.* **2023**, *37*, 100837.
52. Rios, M.; Ponzina, F.; Levisse, A.; Ansaloni, G.; Atienza, D. Bit-Line Computing for CNN Accelerators Co-Design in Edge AI Inference. *IEEE Trans. Emerg. Top. Comput.* **2023**, *11*, 358–372.

53. Tirelli, C.; Sapriza, J.; Alvarez, R.P.; Ferretti, L.; Denking, B.; Ansaloni, G.; Calero, J.M.; Atienza, D.; Pozzi, L. SAT-based Exact Modulo Scheduling Mapping for Resource-Constrained CGRAs. *ACM J. Emerg. Technol. Comput. Syst.* **2024**, *20*, 8.
54. Wang, R.X.; Moon, S.H.; Hu, X.S.; Jiao, X.; Reis, D. A Computing-in-Memory-Based One-Class Hyperdimensional Computing Model for Outlier Detection. *IEEE Trans. Comput.* **2024**, *73*, 1559–1574.
55. Kurungadan, B.; Abdrabou, A. Using Software-Defined Networking for Data Traffic Control in Smart Cities with WiFi Coverage. *Symmetry* **2022**, *14*, 2053.
56. Demirezen, M.U.; Navruz, T.S. Performance Analysis of Lambda Architecture-Based Big-Data Systems on Air/Ground Surveillance Application with ADS-B Data. *Sensors* **2023**, *23*, 7580.
57. Freire, P.; Srivallapanondh, S.; Spinnler, B.; Napoli, A.; Costa, N.; Prilepsky, J.E.; Turitsyn, S.K. Computational Complexity Optimization of Neural Network-Based Equalizers in Digital Signal Processing: A Comprehensive Approach. *J. Light. Technol.* **2024**, *42*, 4177–4201.
58. Zografopoulos, I.; Ospina, J.; Liu, X.R.; Konstantinou, C. Cyber-Physical Energy Systems Security: Threat Modeling, Risk Assessment, Resources, Metrics, and Case Studies. *IEEE Access* **2021**, *9*, 29775–29818.
59. Ling, M.; Feng, Z.H.; Chen, R.Q.; Shao, Y.; Tang, S.D.; Zhu, Y.X. Vina-FPGA-Cluster: Multi-FPGA Based Molecular Docking Tool With High-Accuracy and Multi-Level Parallelism. *IEEE Trans. Biomed. Circuits Syst.* **2024**, *18*, 1321–1337.
60. Li, Z.D.; Shang, C.Q.; Wu, J.J.; Li, Y. Microservice extraction based on knowledge graph from monolithic applications. *Inf. Softw. Technol.* **2022**, *150*, 106992.
61. Nithyoosha, T.; Christopher, P.R. A survey on motion estimation and de-hazing algorithms and architectures. *Digit. Signal Process.* **2023**, *140*, 104130.
62. De Simone, L.; Di Mauro, M.; Natella, R.; Postiglione, F. Performance and Availability Challenges in Designing Resilient 5G Architectures. *IEEE Trans. Netw. Serv. Manag.* **2024**, *21*, 5291–5303.
63. Heideker, A.; Kamienski, C. Network Queuing Assessment: A Method to Detect Bottlenecks in Service Function Chaining. *IEEE Trans. Netw. Serv. Manag.* **2022**, *19*, 4650–4661.
64. Weiss, K.; Rottleuthner, M.; Schmidt, T.C.; Wählich, M. PHiLIP on the HiL: Automated Multi-Platform OS Testing With External Reference Devices. *ACM Trans. Embed. Comput. Syst.* **2021**, *20*, 91.
65. Chatterjee, R.; Paluh, J.L.L.; Chowdhury, S.; Mondal, S.; Raha, A.; Mukherjee, A. SyNC, a Computationally Extensive and Realistic Neural Net to Identify Relative Impacts of Synaptopathy Mechanisms on Glutamatergic Neurons and Their Networks in Autism and Complex Neurological Disorders. *Front. Cell. Neurosci.* **2021**, *15*, 674030.
66. Arney, D.; Zhang, Y.; Kennedy-Metz, L.R.; Dias, R.D.; Goldman, J.M.; Zenati, M.A. An Open-Source, Interoperable Architecture for Generating Real-Time Surgical Team Cognitive Alerts from Heart-Rate Variability Monitoring. *Sensors* **2023**, *23*, 3890.
67. Brohet, M.; Regazzoni, F. A Survey on Thwarting Memory Corruption in RISC-V. *ACM Comput. Surv.* **2024**, *56*, 28.
68. Kim, J.; Kim, E.; Jeon, S.; Ahn, J.; Jun, H.; Cha, H. PVoT: Reconfigurable Photovoltaic Array for Indoor Light Energy-Powered Batteryless Devices. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2022**, *41*, 4181–4192.
69. Fu, Y.R.; Zhang, Y.; Zhu, Q.; Dai, H.N.; Li, M.M.; Quek, T.Q.S. A New Vision of Wireless Edge Caching Networks (WECNs): Issues, Technologies, and Open Research Trends. *IEEE Netw.* **2024**, *38*, 247–253.
70. Jiang, Z.; Dai, X.T.; Burns, A.; Audsley, N.; Gu, Z.H.; Gray, I. A High-Resilience Imprecise Computing Architecture for Mixed-Criticality Systems. *IEEE Trans. Comput.* **2023**, *72*, 29–42.
71. Babun, L.; Aksu, H.; Uluagac, A.S. CPS Device-Class Identification via Behavioral Fingerprinting: From Theory to Practice. *IEEE Trans. Inf. Forensics Secur.* **2021**, *16*, 2413–2428.
72. Fasfous, N.; Vemparala, M.R.; Frickenstein, A.; Valpreda, E.; Salihu, D.; Doan, N.A.V.; Unger, C.; Nagaraja, N.S.; Martina, M.; Stechele, W. HW-FlowQ: A Multi-Abstraction Level HW-CNN Co-design Quantization Methodology. *ACM Trans. Embed. Comput. Syst.* **2021**, *20*, 66.
73. Zhu, Y.Y.; Wei, S.J.; Tiwari, M. Revisiting Browser Performance Benchmarking From an Architectural Perspective. *IEEE Comput. Archit. Lett.* **2022**, *21*, 113–116.
74. Ikhlass, H.; Benjamin, D.; Vincent, C.; Hicham, M. Recent implications towards sustainable and energy efficient AI and big data implementations in cloud-fog systems: A newsworthy inquiry. *J. King Saud Univ.-Comput. Inf. Sci.* **2022**, *34*, 8867–8887.
75. Memis, S.; Yeniceri, R. Model-Based FPGA Implementation of a 6-DoF Dynamical Model Accelerator. *IEEE Access* **2024**, *12*, 45279–45298.
76. Gaffurini, M.; Flammini, A.; Ferrari, P.; Carvalho, D.F.; Godoy, E.P.; Sisinni, E. End-to-End Emulation of LoRaWAN Architecture and Infrastructure in Complex Smart City Scenarios Exploiting Containers. *Sensors* **2024**, *24*, 2024.
77. Li, C.X.; Fan, X.Y.; Wu, X.T.; Yang, Z.; Wang, M.; Zhang, M.; Zhang, S.B. Memory-Computing Decoupling: A DNN Multitasking Accelerator With Adaptive Data Arrangement. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2022**, *41*, 4112–4123.
78. Wu, J.F.; Xu, M.X.; He, Y.Y.; Ye, K.J.; Xu, C.Z. Cloudnativesim: A Toolkit for Modeling and Simulation of Cloud-Native Applications. *Softw. Pract. Exp.* **2025**, *55*, 1185–1208.

79. Pudi, D.; Yang, Y.; Stathis, D.; Prajapati, S.K.; Boppu, S.; Hemani, A.; Cenkeramaddi, L.R. Application Level Synthesis: Creating Matrix-Matrix Multiplication Library: A Case Study. *IEEE Access* **2024**, *12*, 155885–155903.
80. Rafiev, A.; Yakovlev, A.; Tarawneh, G.; Naylor, M.F.; Moore, S.W.; Thomas, D.B.; Bragg, G.M.; Vousden, M.L.; Brown, A.D. Synchronization in graph analysis algorithms on the Partially Ordered Event-Triggered Systems many-core architecture. *IET Comput. Digit. Tech.* **2022**, *16*, 71–88.
81. Guevara, L.M.M.; Vidal, P.J.; Olivera, A.C.; Millán, E.N. Analysis and comparison of encryption and verification algorithms applied to a Fog Computing Architecture. *J. Inf. Telecommun.* **2024**, *9*, 173–189.
82. Uzun, H.; Kavun, E.B. NLU-V: A Family of Instruction Set Extensions for Efficient Symmetric Cryptography on RISC-V. *Cryptography* **2024**, *8*, 9.
83. Goodwill, J.M.; Prasad, N.; Hoskins, B.D.; Daniels, M.W.; Madhavan, A.; Wan, L.; Santos, T.S.; Tran, M.; Katine, J.A.; Braganca, P.M.; et al. Implementation of a Binary Neural Network on a Passive Array of Magnetic Tunnel Junctions. *Phys. Rev. Appl.* **2022**, *18*, 14039.
84. Fé, I.; Nguyen, T.A.; Di Mauro, M.; Postiglione, F.; Ramos, A.; Soares, A.; Choi, E.; Min, D.G.; Lee, J.W.; Silva, F.A. Energy-aware dynamic response and efficient consolidation strategies for disaster survivability of cloud microservices architecture. *Computing* **2024**, *106*, 2737–2783.
85. Djomo, A.F.; Tiedeu, A.; Fotsing, J. Design and implementation in an Altera's cyclone IV EP4CE6E22C8 FPGA board of a fast and robust cipher using combined 1D maps. *IET Image Process.* **2024**, *18*, 1823–1843.
86. Reddi, V.J.; Cheng, C.; Kanter, D.; Mattson, P.; Schmuelling, G.; Wu, C.J. The Vision Behind MLPerf: Understanding AI Inference Performance. *IEEE Micro* **2021**, *41*, 10–18.
87. Xin, Y.; Li, W.J.; Jia, C.J.; Li, X.F.; Xu, Y.; Liu, B.; Tian, Z.H.; Zhang, W.Z. Recursive Multi-Tree Construction With Efficient Rule Sifting for Packet Classification on FPGA. *IEEE/ACM Trans. Netw.* **2024**, *32*, 1707–1722.
88. Jurgielewicz, P.; Fiutowski, T.; Kublik, E.; Skoczen, A.; Szypulska, M.; Wiacek, P.; Hottowy, P.; Mindur, B. Modular Data Acquisition System for Recording Activity and Electrical Stimulation of Brain Tissue Using Dedicated Electronics. *Sensors* **2021**, *21*, 4423.
89. Iwendi, C.; Rehman, S.U.; Javed, A.R.; Khan, S.; Srivastava, G. Sustainable Security for the Internet of Things Using Artificial Intelligence Architectures. *ACM Trans. Internet Technol.* **2021**, *21*, 73.
90. Guler, E.; Karakus, M.; Ayaz, F. Genetic algorithm enabled virtual multicast tree embedding in Software-Defined Networks. *J. Netw. Comput. Appl.* **2023**, *209*, 103538.
91. Laxmisagar, H.S.; Hanumantharaju, M.C. FPGA implementation of breast cancer detection using SVM linear classifier. *Multimed. Tools Appl.* **2023**, *82*, 41105–41128.
92. Bandara, E.; Shetty, S.; Tosh, D.; Liang, X.P. Vind: A Blockchain-Enabled Supply Chain Provenance Framework for Energy Delivery Systems. *Front. Blockchain* **2021**, *4*, 607320.
93. Liu, C.X.; Sabu, A.; Chaudhari, A.; Kang, Q.X.; Carlson, T.E. Pac-Sim: Simulation of Multi-threaded Workloads using Intelligent, Live Sampling. *ACM Trans. Archit. Code Optim.* **2024**, *21*, 81.
94. Murali, P.; Debroy, D.M.; Brown, K.R.; Martonosi, M. Toward Systematic Architectural Design of Near-Term Trapped Ion Quantum Computers. *Commun. ACM* **2022**, *65*, 101–109.
95. Qin, T.; Li, C.; Liu, G.F. Control infrastructure monitoring system at the NSRL facility cluster. *J. Instrum.* **2022**, *17*, P11005.
96. Li, H.Y.; Lu, H.; Li, X.W. Mortar-FP8: Morphing the Existing FP32 Infrastructure for High-Performance Deep Learning Acceleration. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2024**, *43*, 878–891.
97. Charitopoulos, G.; Papaefstathiou, I.; Pnevmatikatos, D.N. Creating Customized CGRAs for Scientific Applications. *Electronics* **2021**, *10*, 445.
98. Pazzaglia, P.; Maggio, M. Characterizing the Effect of Deadline Misses on Time-Triggered Task Chains. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2022**, *41*, 3957–3968.
99. Kohyarnjadfard, I.; Aloise, D.; Dagenais, M.R.; Shakeri, M. A Framework for Detecting System Performance Anomalies Using Tracing Data Analysis. *Entropy* **2021**, *23*, 1011.
100. Das Robin, D.; Khan, J.I. An open-source P416 compiler backend for reconfigurable match-action table switches: Making networking innovation accessible. *Comput. Netw.* **2024**, *242*, 110246.
101. Baazaoui, M.K.; Ketata, I.; Fakhfakh, A.; Derbel, F. Modeling of Packet Error Rate Distribution Based on Received Signal Strength Indications in OMNeT plus plus for Wake-Up Receivers. *Sensors* **2023**, *23*, 2394.
102. Fanti, A.; Perez, C.C.; Denis-Courmont, R.; Roascio, G.; Ekberg, J.E. Toward Register Spilling Security Using LLVM and ARM Pointer Authentication. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2022**, *41*, 3757–3766.
103. Ignatius, T.M.; Singha, T.B.; Palathinkal, R.P. Power Side-Channel Attacks on Crypto-Core Based on RISC-V ISA for High-Security Applications. *IEEE Access* **2024**, *12*, 150230–150248.
104. Horne, R.; Mauw, S.; Mizera, A.; Stemper, A.; Thoemel, J. Anomaly Detection Using Deep Learning Respecting the Resources on Board a CubeSat. *J. Aerosp. Inf. Syst.* **2023**, *20*, 859–872.

105. P., S.; Kavin, B.P.; Srividhya, S.R.; V., R.; C., K.; Lai, W.-C. Performance Evaluation of Stateful Firewall-Enabled SDN with Flow-Based Scheduling for Distributed Controllers. *Electronics* **2022**, *11*, 3000.
106. Aslanpour, M.S.; Toosi, A.N.; Cheema, M.A.; Chhetri, M.B.; Salehi, M.A. Load balancing for heterogeneous serverless edge computing: A performance-driven and empirical approach. *Future Gener. Comput. Syst.* **2024**, *154*, 266–280.
107. Lopez, A.B.; Jin, W.L.; Al Faruque, M.A. Attack Modeling Methodology and Taxonomy for Intelligent Transportation Systems. *IEEE Trans. Intell. Transp. Syst.* **2022**, *23*, 13255–13264.
108. Karim, M.; Khalid, S.; Aleryani, A.; Khan, J.; Ullah, I.; Ali, Z. Human Action Recognition Systems: A Review of the Trends and State-of-the-Art. *IEEE Access* **2024**, *12*, 36372–36390.
109. Torrese, G.; Moriceau, P. An Analytical Approach to Compute the System Architectural Complexity. *IEEE Syst. J.* **2023**, *17*, 3172–3182.
110. Dangl, T.; Sentanoe, S.; Reiser, H.P. Active and passive virtual machine introspection on AMD and ARM processors. *J. Syst. Archit.* **2024**, *149*, 103101.
111. Baumann, C.; Martinoli, A. A modular functional framework for the design and evaluation of multi-robot navigation. *Robot. Auton. Syst.* **2021**, *144*, 103849.
112. Dekhovich, A.; Tax, D.M.J.; Sluiter, M.H.F.; Bessa, M.A. Neural network relief: A pruning algorithm based on neural activity. *Mach. Learn.* **2024**, *113*, 2597–2618.
113. Amponis, G.; Lagkas, T.; Sarigiannidis, P.; Vitsas, V.; Fouliras, P. Inter-UAV Routing Scheme Testbeds. *Drones* **2021**, *5*, 2.
114. Huzaifa, M.; Desai, R.; Grayson, S.; Jiang, X.T.; Jing, Y.; Lee, J.; Lu, F.; Pang, Y.H.; Ravichandran, J.; Sinclair, F.; et al. ILLIXR: An Open Testbed to Enable Extended Reality Systems Research. *IEEE Micro* **2022**, *42*, 97–106.
115. Jiang, Z.; Yang, K.C.; Fisher, N.; Audsley, N.; Dong, Z. Towards an energy-efficient quarter-clairvoyant mixed-criticality system. *J. Syst. Archit.* **2022**, *130*, 102683.
116. Sgherzi, F.; Siracusa, M.; Fernandez, I.; Armejach, A.; Moretó, M. SpChar: Characterizing the sparse puzzle via decision trees. *J. Parallel Distrib. Comput.* **2024**, *192*, 104941.
117. Xu, Y.Q.; Li, B.Y.; Zhu, Z.W.; Liu, W.H.; Jia, G.Y.; Han, G.J.; Li, X. MultiRuler: A Multi-Dimensional Resource Modeling Method for Embedded Intelligent Systems of Autonomous Driving. *IEEE Trans. Veh. Technol.* **2024**, *73*, 6212–6224.
118. Charitopoulos, G.; Pnevmatikatos, D.N.; Gaydadjiev, G. MC-DeF: Creating Customized CGRAs for Dataflow Applications. *ACM Trans. Archit. Code Optim.* **2021**, *18*, 26.
119. Arroqui, M.; Ferreira, F.; Roselli, M.; Alvarez, J.R.; Machado, C.; Mateos, C.; Zunino, A. A Simulation Scheduling Module to Improve User Experience in the Simugan Beef-Cattle Farm Simulator. *IEEE Lat. Am. Trans.* **2022**, *20*, 162–170.
120. Challita, F.; Liénard, M.; Gaillot, D.P.; Molina-Garcia-Pardo, J.M. Evaluation of an Antenna Selection Strategy for Reduced Massive MIMO Complexity. *Radio Sci.* **2021**, *56*, e2020RS007242.
121. Johnson, J.; Boxer, B.; Prakash, T.; Grace, C.; Sorensen, P.; Tripathi, M. Investigating resource-efficient neutron/gamma classification ML models targeting eFPGAs. *J. Instrum.* **2024**, *19*, P07034.
122. Schoonhoven, R.A.; van Werkhoven, B.; Batenburg, K.J. Benchmarking Optimization Algorithms for Auto-Tuning GPU Kernels. *IEEE Trans. Evol. Comput.* **2023**, *27*, 550–564.
123. da Silva, C.A.C.F.; Rosa, D.C.; Miranda, P.B.C.; Si, T.P.; Cerri, R.; Basgalupp, M.P. Automated CNN optimization using multi-objective grammatical evolution. *Appl. Soft Comput.* **2024**, *151*, 111124.
124. Caforio, A.; Banik, S.; Todo, Y.; Meier, W.; Isobe, T.; Liu, F.K.; Zhang, B. Perfect Trees: Designing Energy-Optimal Symmetric Encryption Primitives. *IACR Trans. Symmetric Cryptol.* **2021**, *2021*, 36–73.
125. Rojas-Muñoz, L.F.; Sánchez-Solano, S.; Martínez-Rodríguez, M.C.; Brox, P. On-Line Evaluation and Monitoring of Security Features of an RO-Based PUF/TRNG for IoT Devices. *Sensors* **2023**, *23*, 4070.
126. de Lima, E.C.; Rossi, F.D.; Luizelli, M.C.; Calheiros, R.N.; Lorenzon, A.F. A neural network framework for optimizing parallel computing in cloud servers. *J. Syst. Archit.* **2024**, *150*, 103131.
127. Alabdulatif, A.; Khalil, I.; Rahman, M.S. Security of Blockchain and AI-Empowered Smart Healthcare: Application-Based Analysis. *Appl. Sci.* **2022**, *12*, 11039.
128. Kumar, A.S.; Reddy, B.N.K. An Efficient Real-Time Embedded Application Mapping for NoC Based Multiprocessor System on Chip. *Wirel. Pers. Commun.* **2023**, *128*, 2937–2952.
129. Toreini, E.; Mehrnezhad, M.; van Moorsel, A. Fairness as a Service (FaaS): Verifiable and privacy-preserving fairness auditing of machine learning systems. *Int. J. Inf. Secur.* **2024**, *23*, 981–997.
130. Tang, L.; Wang, K.; Zhang, Y.; Zhou, X.L.; Chen, Q.B. Service Function Chain Anomaly Detection Based on Distributed Generative Adversarial Network in Network Slicing Scenario. *J. Electron. Inf. Technol.* **2023**, *45*, 262–271.
131. Muro, F.; Baena, E.; Fortes, S.; Nielsen, L.; Barco, R. Noisy Neighbour Impact Assessment and Prevention in Virtualized Mobile Networks. *IEEE Trans. Netw. Serv. Manag.* **2023**, *20*, 415–425.
132. Ramasubramanian, A.K.; Kazasidis, M.; Fay, B.; Papakostas, N.; Doulamis, A. On the Evaluation of Diverse Vision Systems towards Detecting Human Pose in Collaborative Robot Applications. *Sensors* **2024**, *24*, 578.

133. Upadhyaya, P.S.; Tripathi, N.; Gaedert, J.; Reed, J.H. Open AI Cellular (OAIC): An Open Source 5G O-RAN Testbed for Design and Testing of AI-Based RAN Management Algorithms. *IEEE Netw.* **2023**, *37*, 7–15.
134. Zafar, S.; Ayub, U.; Alkhamash, H.I.; Ullah, N. Framework for Efficient Auto-Scaling of Virtual Network Functions in a Cloud Environment. *Sensors* **2022**, *22*, 7597.
135. Xu, R.; Sha, E.H.M.; Zhuge, Q.F.; Song, Y.H.; Wang, H.; Shi, L. Optimizing Data Placement for Hybrid SRAM plus Racetrack Memory SPM in Embedded Systems. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2023**, *42*, 847–859.
136. Dipu, M.T.A.; Hossain, S.S.; Arafat, Y.; Rafiq, F.B. Real-time Driver Drowsiness Detection using Deep Learning. *Int. J. Adv. Comput. Sci. Appl.* **2021**, *12*, 844–850.
137. da Silva, M.A.; Garcia, R.D.; Carlo, J.C. Multi-objective optimization algorithms for building performance assessment—A benchmark. *Int. J. Archit. Comput.* **2024**, *24*, 35–59.
138. Nguyen, M.T.; Truong, H.L. On Optimizing Resources for Real-Time End-to-End Machine Learning in Heterogeneous Edges. *Softw. Pract. Exp.* **2025**, *55*, 541–558.
139. Lee, W.; Lee, J.; Park, B.K.; Kim, R.Y.C. Microarchitectural Characterization on a Mobile Workload. *Appl. Sci.* **2021**, *11*, 1225.
140. Crisci, L.; Carpentieri, L.; Cosenza, B.; Accordi, G.; Gadioli, D.; Vitali, E.; Palermo, G.; Beccari, A.R. Enabling performance portability on the LiGen drug discovery pipeline. *Future Gener. Comput. Syst.* **2024**, *158*, 44–59.
141. Chowdhury, R.; Talhi, C.; Ould-Slimane, H.; Mourad, A. Proactive and Intelligent Monitoring and Orchestration of Cloud-Native IP Multimedia Subsystem. *IEEE Open J. Commun. Soc.* **2024**, *5*, 139–155.
142. Borylo, P.; Davoli, G.; Rzepka, M.; Lason, A.; Cerroni, W. Unified and standalone monitoring module for NFV/SDN infrastructures. *J. Netw. Comput. Appl.* **2021**, *175*, 102934.
143. Jha, A.V.; Appasani, B.; Ghazali, A.; Bizon, N. A Comprehensive Risk Assessment Framework for Synchrophasor Communication Networks in a Smart Grid Cyber Physical System with a Case Study. *Energies* **2021**, *14*, 3428.
144. Cheng, J.W.; Jiang, X.Y.; Zhou, H.L.; Dong, J.J. Advances and Challenges of Optoelectronic Intelligent Computing. *Chin. J. Lasers* **2022**, *49*, 1219001.
145. Mukhopadhyay, N.; Tewari, B.P. Cost and energy aware migration through dependency analysis of VM components in virtual cloud infrastructure. *Computing* **2025**, *107*, 24.
146. Napoli, O.; Duarte, D.; Alves, P.; Soto, D.H.P.; de Oliveira, H.E.; Rocha, A.; Boccato, L.; Borin, E. A benchmark for domain adaptation and generalization in smartphone-based human activity recognition. *Sci. Data* **2024**, *11*, 1192.
147. Xu, T.N.; Sun, H.F.; Zhang, D.; Zhou, X.M.; Sui, X.F.; Wang, S.; Huang, Q.; Bao, Y.G. NfvInsight: A Framework for Automatically Deploying and Benchmarking VNF Chains. *J. Comput. Sci. Technol.* **2022**, *37*, 680–698.
148. AlShboul, R.; Khasawneh, A.M.; Al-Rousan, R.; Kumar, A.; Kumar, S.; Kaiwartya, O. D3S-Drone Security Surveillance System for Connected Drone Environment. *Ad Hoc Sens. Wirel. Netw.* **2023**, *57*, 209–225.
149. Parks, Z.; Carignan-Dugas, A.; Gustafson, E.; Meurice, Y.; Dreher, P. Applying the noiseless extrapolation error mitigation protocol to calculate real-time quantum field theory scattering phase shifts. *Phys. Rev. D* **2024**, *109*, 14505.
150. Zhang, Q.; Liu, Y.; Liu, T. iBalancer: Load-Aware in-Server Flow Scheduling for Sub-Millisecond Tail Latency. *IEEE Trans. Parallel Distrib. Syst.* **2022**, *33*, 1761–1774.
151. Agrawal, N. Autonomic cloud computing based management and security solutions: State-of-the-art, challenges, and opportunities. *Trans. Emerg. Telecommun. Technol.* **2021**, *32*, e4349.
152. Guo, P.F.; Yan, Y.J.; Zhang, F.; Zhu, C.S.; Zhang, L.C.; Dai, Z.B. Extending the classical side-channel analysis framework to access-driven cache attacks. *Comput. Secur.* **2023**, *129*, 103255.
153. Lin, M.M.; Zhang, L.W.; Wang, Z.B.; Liu, H.Y.; Wang, K.Q.; Tang, G.Z.; Wang, W.K.; Sun, P. A combined system with convolutional neural networks and transformers for automated quantification of left ventricular ejection fraction from 2D echocardiographic images. *Intell. Med.* **2025**, *5*, 46–53.
154. Zaghloul, M.; Salem, M.; Ali-Eldin, A. A new framework based on features modeling and ensemble learning to predict query performance. *PLoS ONE* **2021**, *16*, e0258439.
155. Benavides-López, J.A.; Rodríguez-Bulnes, J.; Collazo, J.R. Workflow for high definition documentation of the roman archaeological site of Herrera (Seville). *Disegnarecon* **2023**, *16*, 2.1–2.10.
156. Garcia, L.; Vazquez, E.; Sanchez, G.; Avalos, J.G.; Sanchez, G. An ultra-compact and high-speed FFT-based large-integer multiplier for fully homomorphic encryption using a dual spike-based arithmetic circuit over GF(p). *Neurocomputing* **2022**, *507*, 54–66.
157. Martínez-Ruedas, C.; Adame-Rodríguez, F.J.; Díaz-Cabrera, J.M. Integrating and interconnecting of older SINUMERIK CNC machines with industry 4.0 using a plug-and-play system. *J. Ind. Inf. Integr.* **2024**, *38*, 100583.
158. Morell, J.A.; Dahi, Z.A.; Chicano, F.; Luque, G.; Alba, E. A multi-objective approach for communication reduction in federated learning under devices heterogeneity constraints. *Future Gener. Comput. Syst.* **2024**, *155*, 367–383.
159. Sheraz, S.M.; Arfeen, A.; Haider, U. Energy-Efficient Data Center Network Infrastructure With Network Switch Refresh Model. *IEEE Access* **2023**, *11*, 45066–45082.

160. Costanzo, M.; Rucci, E.; García-Sánchez, C.; Naiouf, M. Viability Study of SYCL as a Unified Programming Model for Heterogeneous Systems Based on GPUs in Bioinformatics. *J. Comput. Sci. Technol.* **2024**, *24*, 193–194.
161. Kaiser, S.; Tosun, A.S.; Korkmaz, T. Benchmarking Container Technologies on ARM-Based Edge Devices. *IEEE Access* **2023**, *11*, 107331–107347.
162. Perrelli, M.; Cosco, F.; Carbone, G.; Lenzo, B.; Mundo, D. On the Benefits of Using Object-Oriented Programming for the Objective Evaluation of Vehicle Dynamic Performance in Concurrent Simulations. *Machines* **2021**, *9*, 41.
163. Abed, S.; Jaffal, R.; Mohd, B.J.; Al-Shayegi, M. An analysis and evaluation of lightweight hash functions for blockchain-based IoT devices. *Clust. Comput.* **2021**, *24*, 3065–3084.
164. Deshpande, P.; Kothari, A.G. Triple DES with radial basis function networks for securing in process of CCTV footage images. *Comput. Inform.* **2024**, *43*, 633–666.
165. Nizamani, A.H.; Chen, Z.G.; Nizamani, A.A.; Bhatti, U.A. Advance brain tumor segmentation using feature fusion methods with deep U-Net model with CNN for MRI data. *J. King Saud Univ.-Comput. Inf. Sci.* **2023**, *35*, 101793.
166. Beskopylny, A.N.; Stel'makh, S.A.; Shcherban', E.M.; Razveeva, I.; Kozhakin, A.; Meskhi, B.; Chernil'nik, A.; Elshaeva, D.; Ananova, O.; Giry, M.; et al. Computer Vision Method for Automatic Detection of Microstructure Defects of Concrete. *Sensors* **2024**, *24*, 4373.

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